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Description

[METHOD OF FABRICATING FLASH MEMORY]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The invention relates in general to a method of fabricating a flash memory, and more particularly, to a method of a flash memory in which an overlapping area between a floating gate and a control gate is increased.

[0003] Related Art of the Invention

[0004] Flash memory has been broadly applied in personal computer and electronic products due to the superior data retention characteristics.

[0005] The typical flash memory has a stack-gate structure, which comprises a tunneling oxide layer, a polysilicon floating gate used to store charges, a silicon oxide/silicon nitride/silicon oxide (ONO) dielectric layer, and a polysilicon control gate used to control the data access.

[0006] Normally, the larger the gate-coupling ratio (GCR) between the floating gate and the control gate, the lower the operation voltage required. Consequently, operation speed and efficiency are greatly enhanced. The method of increasing the gate-coupling ratio includes increasing the overlap area, the thickness of the dielectric layer, and the dielectric constant k of the dielectric layer between the floating gate and the control gate.

[0007] As mentioned above, increasing the overlap area between the floating gate and the control gate is advantageous to increasing the gate-coupling ratio. However, due to the continuous demand of higher integration, the area occupied by each memory cell has to be reduced. Therefore, how to fabricate a flash memory with a high gate-coupling rate within limited chip area has become an important task.

SUMMARY OF INVENTION

[0008] The present invention provides a method of fabricating a flash memory in which the overlap area between a floating gate and a control gate is increased, such that the coupling ratio thereof is increased.

[0009] The method of fabricating a flash memory provided by the present invention comprises the following steps. A tun-

neling dielectric layer, a conductive layer and a mask layer are sequentially formed on a substrate. The mask layer, the conductive layer and the tunneling dielectric layer are patterned to form longitudinally arranged strips on the substrate. Buried source/drain regions are then formed in the substrate between the strips. The strips are further patterned to form gate structures, which thus respectively comprise one patterned tunneling dielectric layer, one patterned conductive layer and one patterned mask layer. An insulation layer is formed on sideways adjacent to the gate structures. The insulation layer has a top surface at a height lower than a top surface of the patterned conductive layer of the gate structures, such that a part of the sidewalls of the gate structures is exposed. A material layer then is formed on the insulation layer sideways adjacent to the gate structures. The patterned mask layer is removed to expose the top surface of the patterned conductive layer. An additional patterned conductive layer then is formed on the exposed patterned conductive layer in a manner to extend over the sideways adjacent material layer. The additional patterned conductive layer thereby has an area greater than that of the first patterned conductive layer, and forms with this latter a floating gate.

The material layer then is removed, and a gate dielectric layer is formed on the exposed top surface and sidewalls of the floating gates. Lastly, a control gate is formed on the gate dielectric layer.

[0010] In the present invention, the height of the insulation layer formed sideways adjacent to the gate structures is reduced, such that the additional patterned conductive layer formed on the first patterned conductive layer extends over the buried source/drain regions to form a floating gate. As a result, the overlapping area between the control gate and the floating gate is increased, and the gate-coupling ratio is increased.

BRIEF DESCRIPTION OF DRAWINGS

[0011] These, as well as other features of the present invention, will become more apparent upon reference to the following drawings.

[0012] Figures 1A to 1L are top views showing the fabrication process of a flash memory according to an embodiment of the present invention.

[0013] Figures 2A to 2L are cross-sectional views respectively taken along section I-I" of Figures 1A to 1L.

[0014] Figures 3 and 4 are cross-sectional views showing the fabrication process of a flash memory according to an-

other embodiment of the present invention.

DETAILED DESCRIPTION

[0015] Figures 1A to 1L are top views showing the fabrication process of a flash memory according to a preferred embodiment of the present invention. Figures 2A to 2L are cross-sectional views along line I-I" as shown in Figures 1A to 1L, respectively. Referring to Figures 1A and 2A, a substrate 100 is provided. The substrate 100 is, for example, a silicon substrate. A tunneling dielectric layer 102, a conductive layer 104 and a mask layer 106 are sequentially formed on the substrate 100. The material of the tunneling dielectric layer 102 includes silicon oxide, and the thickness thereof is about 50 angstroms to about 100 angstroms, for example.

[0016] The method for forming the tunneling dielectric layer 102 includes thermal oxidation or low-pressure chemical vapor deposition (LPCVD), for example. The material of the conductive layer 104 includes doped polysilicon, which is formed by, for example, performing low-pressure chemical vapor deposition with silane as a gas source to deposit a polysilicon layer, followed by an dopant implantation process. The operation of the deposition process is about 575°C to about 650°C, and the operation pressure thereof

is about 0.3 torr to about 0.6 torr.

[0017] The material of the mask layer 106 includes silicon nitride or silicon oxide. Silicon nitride is formed by, for example, performing a low-pressure chemical vapor deposition using dichloro-silane and ammonia as reacting gases.

[0018] Referring to Figures 1B and 2B, a patterned photoresist layer 108 is formed on the mask layer 106. The mask layer 106, the conductive layer 104 and the tunneling dielectric layer 102 are etched using the patterned photoresist layer 108 as a mask to form a plurality of strips 200 longitudinally arranged on the substrate 100. The strips 200 respectively comprise the patterned tunneling dielectric layer 102a, the patterned conductive layer 104a, and the patterned mask layer 106a. An ion implantation step is performed to form buried source/drain regions 110 in the substrate between the strips 200.

[0019] Referring to Figures 1C and 2C, the patterned photoresist layer 108 is removed. Another patterned photoresist layer (not shown) is formed on the strips, and the strips 200 are etched using the patterned photoresist layer as a mask to form the gate structures 300. The floating gate structures 300 comprise the patterned tunneling dielectric layer 102b, the patterned conductive layer 104b, and the pat-

terned mask layer 106b.

[0020] Referring to Figures 1D and 2D, an insulation layer 112 is formed on the substrate 100 to cover the gate structures 300 and fill the spaces between the gate structures 300. The material for forming the insulation layer 112 has an etching selectivity different from that of the mask layer 106b, and is, for example, silicon oxide, silicon nitride or spin-on-glass material. The method for forming the insulation layer 112 includes, for example, performing a high-density plasma chemical vapor deposition (HDP-CVD) or spin-coating.

[0021] Referring to Figures 1E and 2E, the insulation layer 112 on the mask layer 106b is removed to expose the patterned mask layer 106b. The remaining insulation layer, located sideways adjacent to the gate structures 300, is denoted by reference numeral 112a. The method for partly removing the insulation layer 112 includes, for example, performing a chemical mechanical polishing (CMP) or a back etching.

[0022] Referring to Figures 1F and 2F, a part of the remaining insulation layer 112a is removed to leave a remaining insulation layer 112b with a top surface lower than a top surface of the conductive layer 104b, such that a part of the

sidewall of the conductive layer 104b is exposed. The method for partly removing the insulation layer 112a includes, for example, performing a back etching.

[0023] Referring to Figures 1G and 2G, a material layer 114 is formed on the insulation layer 112b to cover the gate structures 300 and fill the spaces between the gate structures 300. The material of the layer 114 includes, for example, boron-phosphorus silicate glass (BPSG) or phosphorus silicate glass (PSG), and has an etching rate different from those of the mask layer 106b and insulation layer 112b. A material layer 114 made of BPSG is formed by, for example, performing a normal-pressure CVD with silane, hydrogen phosphide, and hydrogen boride as reacting gas sources, and a reaction temperature between about 350°C and 450°C.

[0024] Referring to FIG. 1H and 2H, the material layer 114 on the mask layer 106b is removed to expose the patterned mask layer 106b, which leaves remaining material layer 114a sideways adjacent to the gate structures 300. The method for removing the material layer 114 includes, for example, performing a CMP or back etching.

[0025] Referring to Figures 1I and 2I, the mask layer 106b is removed to expose the top surface of the conductive layer

104b. The method for removing the mask layer 106b includes, for example, performing a wet etching. If the material of the mask layer 106b is silicon nitride, the etchant used in the wet etching step includes, for example, phosphoric acid.

[0026] Referring Figures 1J and 2J, another patterned conductive layer 116 is formed on the patterned conductive layer 104b, and further overlaps a peripheral portion of the material layer 114a. In other words, the patterned conductive layer 116 has an upper surface area greater than that of the patterned conductive layer 104b, and forms with this latter a floating gate 400.

[0027] In an embodiment, the formation of the patterned conductive layer 116 comprises forming a conductive layer, for example, doped polysilicon, over the patterned conductive layer 104b and material layer 114a. Low-pressure CVD, for example, may be performed to form this conductive layer, on which a patterned photoresist layer (not shown) is subsequently formed. Using the patterned photoresist layer as a mask, the conductive layer 116 then is etched to expose the material layer 114a.

[0028] Referring to Figures 1K and 2K, the material layer 114a is removed by, for example, back etching.

[0029] Referring to Figures 1L and 2L, a gate dielectric layer 118 is formed over the substrate to cover the sidewalls of the patterned conductive layer 104b and the top surface and sidewalls of the patterned conductive layer 116. The gate dielectric layer 118 is, for example, silicon oxide/silicon nitride/silicon oxide (ONO). The method for forming the gate dielectric layer 118 includes, for example, forming an oxide layer by thermal oxidation, followed by a low-pressure CVD to respectively form a silicon nitride layer and another silicon oxide layer. The gate dielectric layer 118 also may be made of other materials such as silicon oxide or silicon oxide/silicon nitride.

[0030] A conductive layer 120 is formed on the gate dielectric layer 118, used as a control gate. The conductive layer 120 includes, for example, a policide layer consisting of a doped polysilicon layer 122 and a metal silicide layer 124. The method for forming the doped polysilicon layer 122 includes, for example, performing an in-situ doping step. The metal silicide layer is formed by a method that comprises, for example, performing a low-pressure CVD using metal fluoride and silane as gas sources. The subsequent process for forming the flash memory is known in the art and is not further described.

[0031] As described above, the floating gate is comprised of two patterned conductive layers specifically formed by the invention. A first conductive layer is formed between the buried source/drain regions with sidewalls laterally exposed. A second conductive layer is formed on the first conductive layer in a manner to further extend over the adjacent buried source/drain regions. The overlapping area between the floating gate and the control gate thereby is increased, which favorably increases the device coupling ratio.

[0032] Figure 3 illustrates an intermediary manufacture stage where the processed substrate has undergone the processing steps described in Figures 2A through 2J. Thereafter, a material layer 302 is formed in the spaces between the patterned conductive layer 116. The height of the top surface of the layer 302 is lower or approximately as high as that of the top surface of the patterned conductive layer 116. Another patterned conductive layer 304 is formed on the patterned conductive layer 116. The patterned conductive layer 304 covers the patterned conductive layer 116 and further extends over a peripheral portion of the material layer 302.

[0033] Referring to Figure 4, the material layer 114a and the ma-

terial layer 302 are removed to form a floating gate comprised of the conductive layers 104b, 116, 304. A gate dielectric layer 118 is subsequently formed on the exposed surface of the floating gate. Lastly, a conductive layer 120 is formed on the gate dielectric layer 118, used as control gate.

[0034] To further increase the overlapping area between the floating gate and the control gate, additional conductive layers may be further sequentially formed on the conductive layer 104b by repeating the above processing steps for forming the material layer 302 and conductive layer 304.

[0035] As described above, the height of the insulation layer surrounding the floating gate therefore is reduced in the invention, such that the sidewall of the floating gate is partly exposed, resulting in a larger overlapping area with the control gate. Consequently, the gate-coupling ratio is increased without increasing the cell area of the flash memory.

[0036] Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered

as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.